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Using Programmable Hardware to Improve Performance

Flexible Peripheral Interconnections for Triggering

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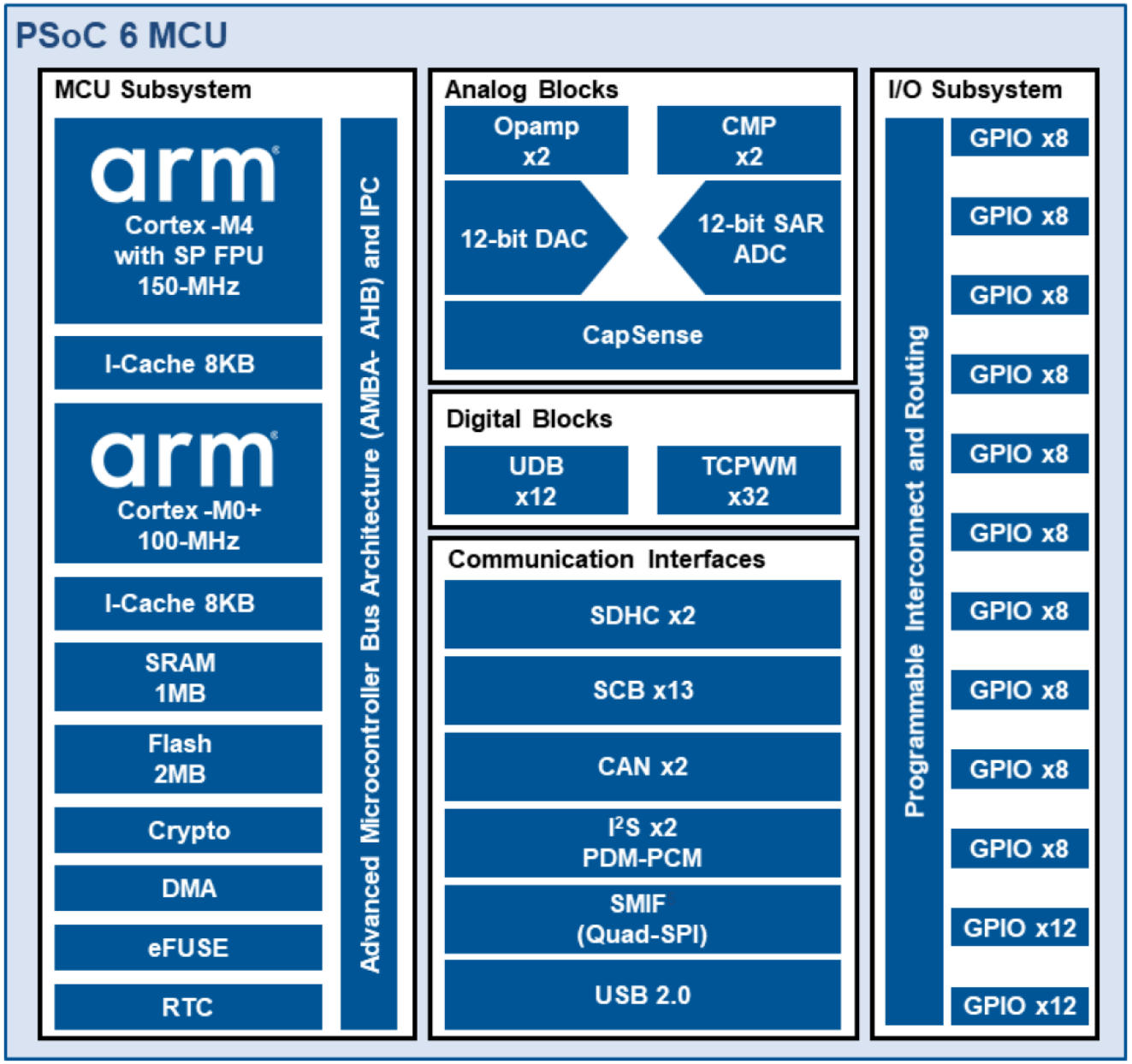
Renesas RL78 Event Link Controller peripheral

Register Name	Event Generator (Output Origin of Event Input n)
ELSELR00	External interrupt edge detection 0
ELSELR01	External interrupt edge detection 1
ELSELR02	External interrupt edge detection 2
ELSELR03	External interrupt edge detection 3
ELSELR04	External interrupt edge detection 4
ELSELR05	External interrupt edge detection 5
ELSELR06	Key return signal detection
ELSELR07	RTC fixed-cycle signal/Alarm match detection
ELSELR08	Timer RD0 input capture A/compare match A
ELSELR09	Timer RD0 input capture B/compare match B
ELSELR10	Timer RD1 input capture A/compare match A
ELSELR11	Timer RD1 input capture B/compare match B
ELSELR12	Timer RD1 underflow
ELSELR13	Timer RJ0 underflow/end of pulse width measurement period/end of pulse period measurement period
ELSELR14	Timer RG input capture A/compare match A
ELSELR15	Timer RG input capture B/compare match B
ELSELR16	TAU channel 00 count end/capture end
ELSELR17	TAU channel 01 count end/capture end
ELSELR18	TAU channel 02 count end/capture end
ELSELR19	TAU channel 03 count end/capture end
ELSELR20 Note 1	TAU channel 10 count end/capture end
ELSELR21 Note 1	TAU channel 11 count end/capture end
ELSELR22 Note 1	TAU channel 12 count end/capture end
ELSELR23 Note 1	TAU channel 13 count end/capture end
ELSELR24 Note 2	Comparator detection 0
ELSELR25 Note 2	Comparator detection 1

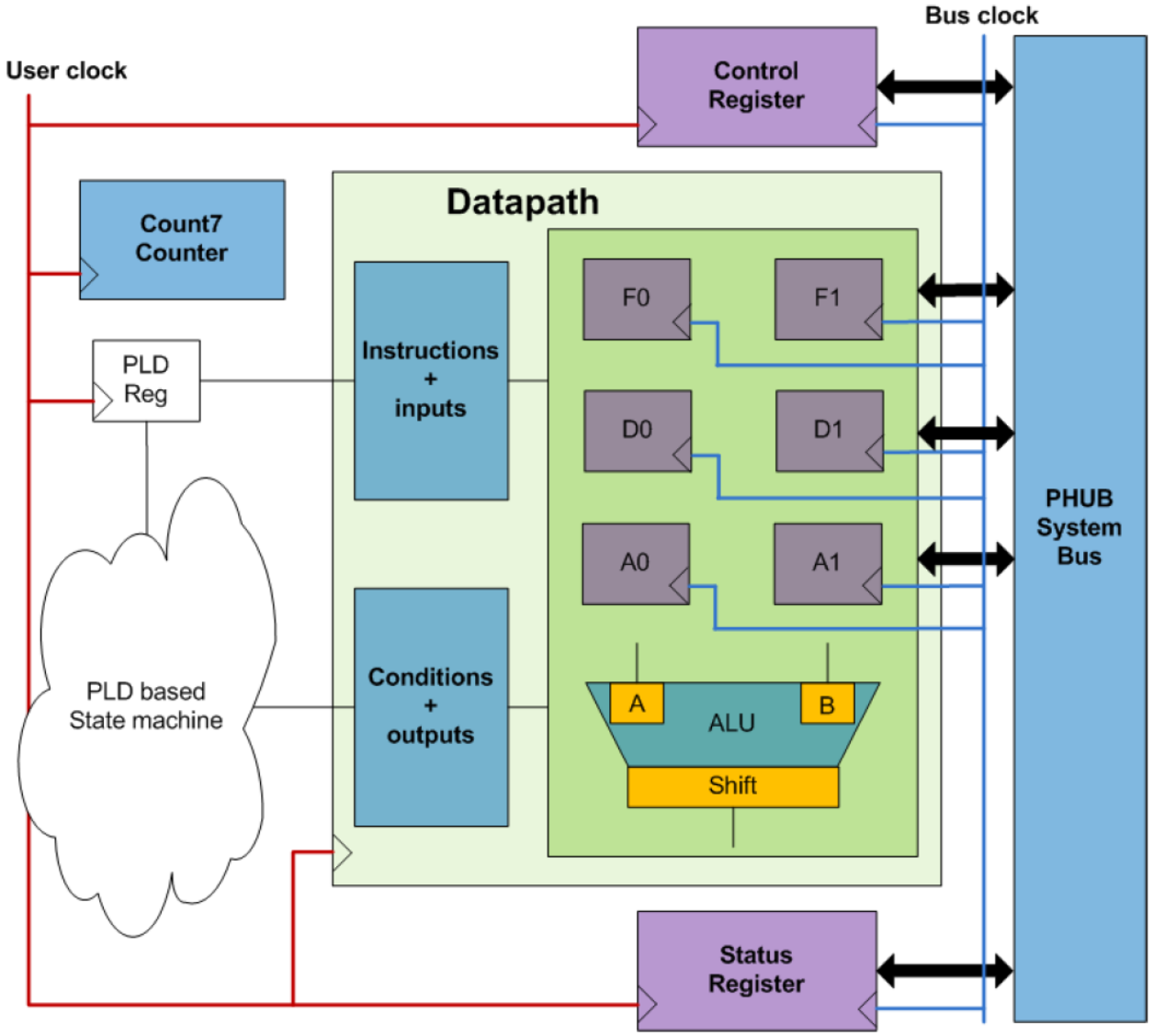
Link Destination Peripheral Function	Operation When Receiving Event
A/D converter	A/D conversion starts
Timer input of timer array unit 0 channel 0 Note 1	Delay counter, input pulse interval measurement, external event counter
Timer input of timer array unit 0 channel 1 Note 2	Delay counter, input pulse interval measurement, external event counter
Timer RJ0	Count source
Timer RG	TRGIOB input capture
Timer RD0	TRDIOD0 input capture, pulse output forced cutoff
Timer RD1	TRDIOD1 input capture, pulse output forced cutoff
DA0 Note 3	Real-time output (96 KB or more code flash memory products only.)
DA1 Note 3	Real-time output (96 KB or more code flash memory products only.)

Cypress PSoC 6 MCU



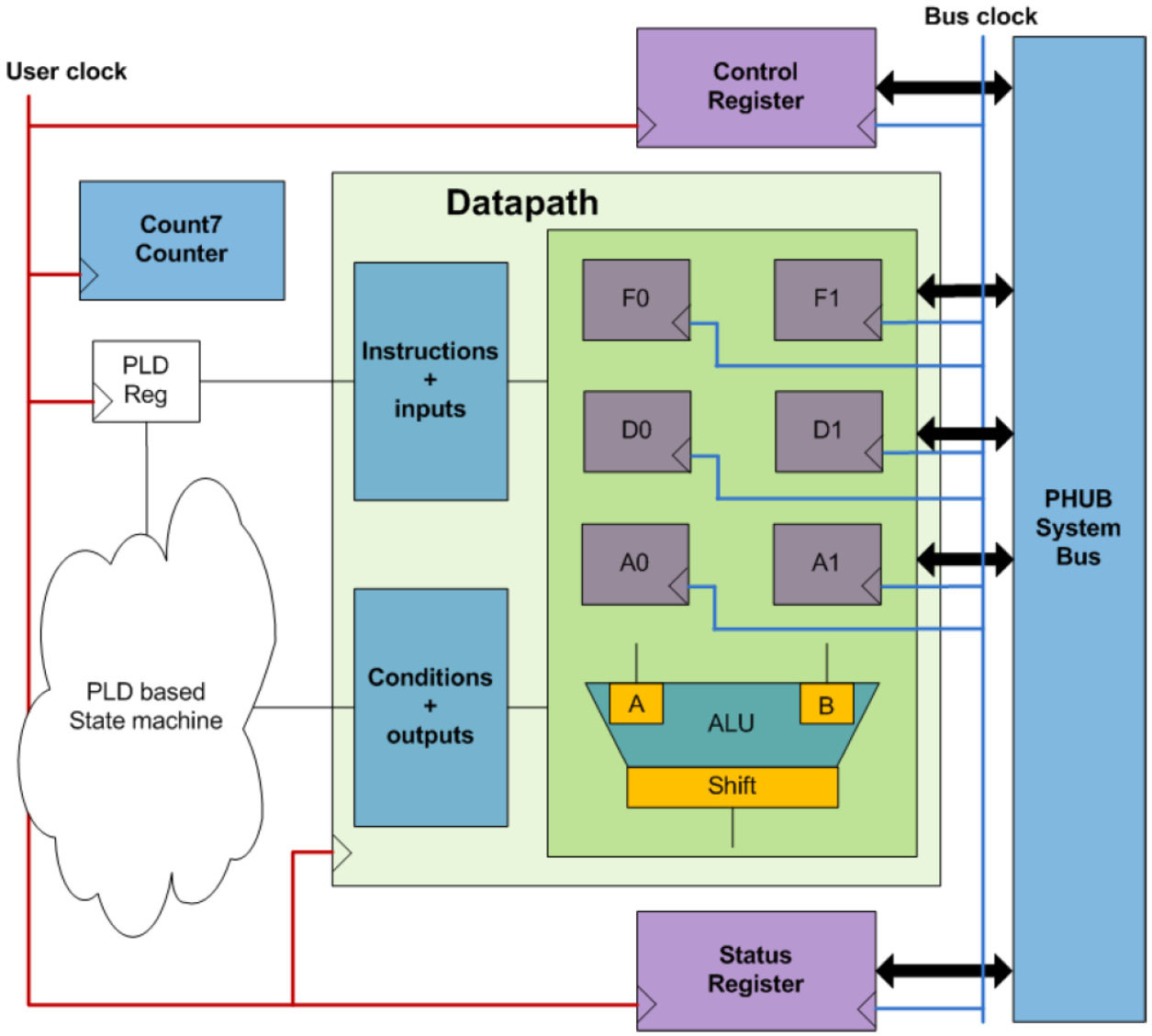
- Dual CPU cores
  - Cortex-M4 @ 150 MHz
  - Cortex-M0+ @ 100 MHz
- On-chip RAM, Flash ROM
- Typical MCU peripherals
  - Digital peripherals
  - GPIO subsystem
  - Communications interfaces
  - Timer/Counter/PWMs
- Programmable digital blocks
- Programmable analog blocks

Universal Digital Block



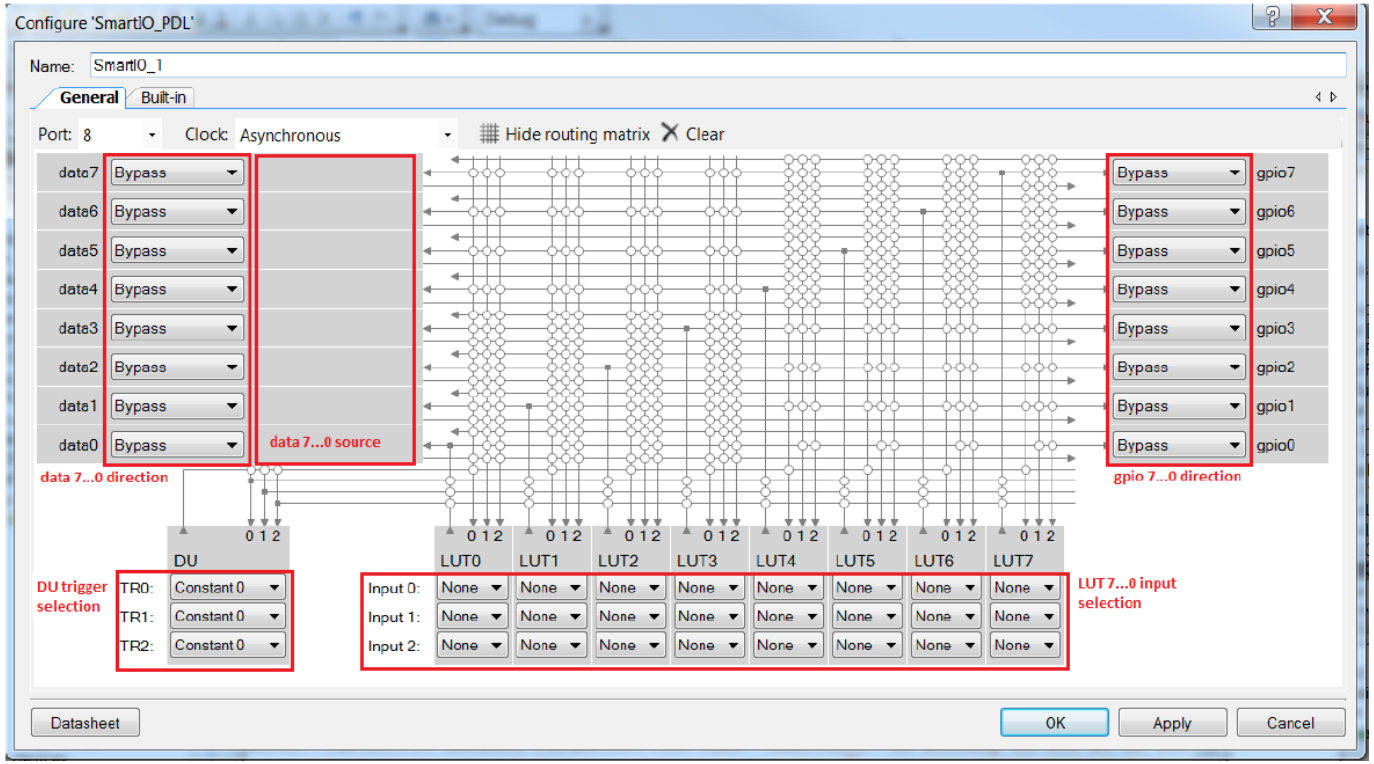
- Used to create synchronous state machines
- Five elements
  - Byte Datapath
  - Two Programmable Logic Devices (PLDs)
  - Byte Control Register
  - Byte Status register
  - Down Counter (7 bits)
- Use as
  - Drag-and-drop Boolean primitives (gates, registers)
  - Verilog programmable blocks
- Cypress-provided peripheral component library using UDBs to implement functions
  - Communication peripherals: LIN, UART, SPI, I2C, S/PDIF and other protocols
  - Waveform Generators
  - Pseudo-Random Sequence (PRS) generation
  - Many other functions

Datapath Element



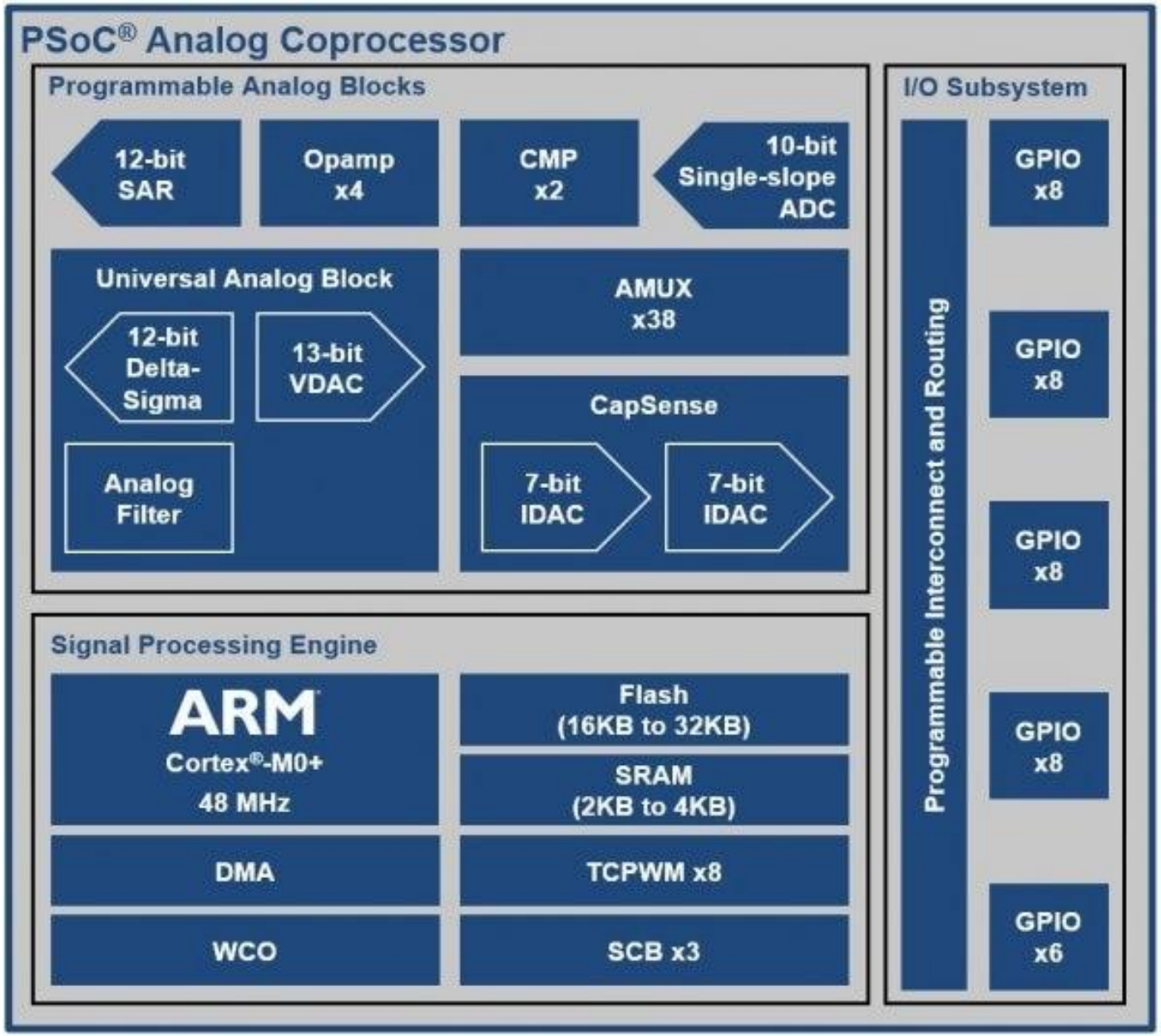
- 8 bits wide, can be paralleled
- Can perform simple arithmetic and bitwise operations
- Up to 8 user-defined instructions
- Programmable ALU
- Accumulator Registers A0, A1
- Data registers D0, D1
- Dual four-entry FIFOs F0, F1
- Shifting function
- Masking Function

Smart I/O Block

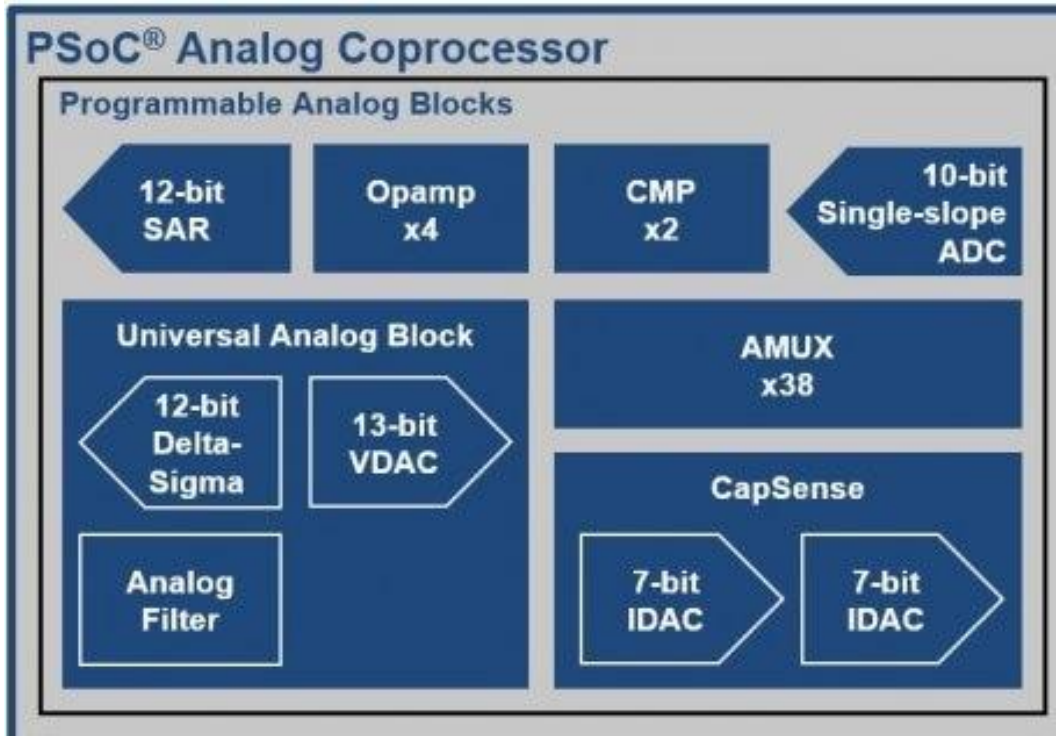


- Programmable logic interconnection system
- Enables Boolean operations on incoming or outgoing signals
- 8 Look-Up Tables
  - 8x1 bit each
  - Can use to implement logic or other functions
- 8-bit Data Unit
  - Three selectable triggers
  - Operations:
    - Count: up, down, up/down. Optional wrap
    - Rotate right, shift right
    - Logic AND, Majority 3, Match Data

Cypress PSoC Analog Coprocessor

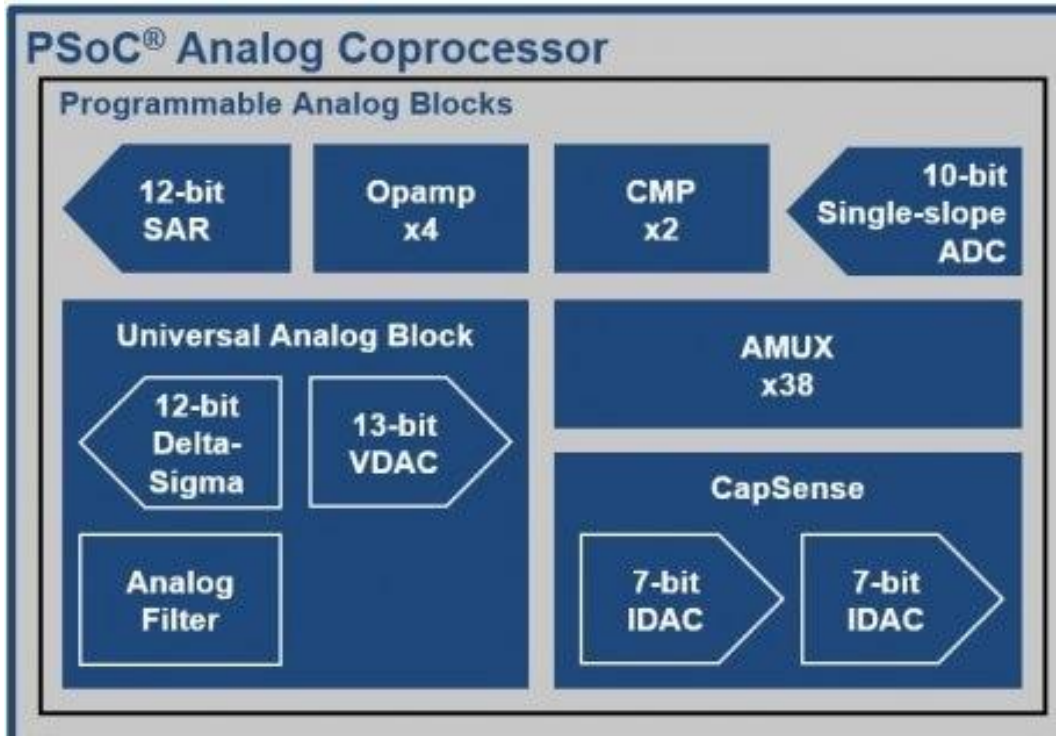


Cypress PSoC Analog Coprocessor



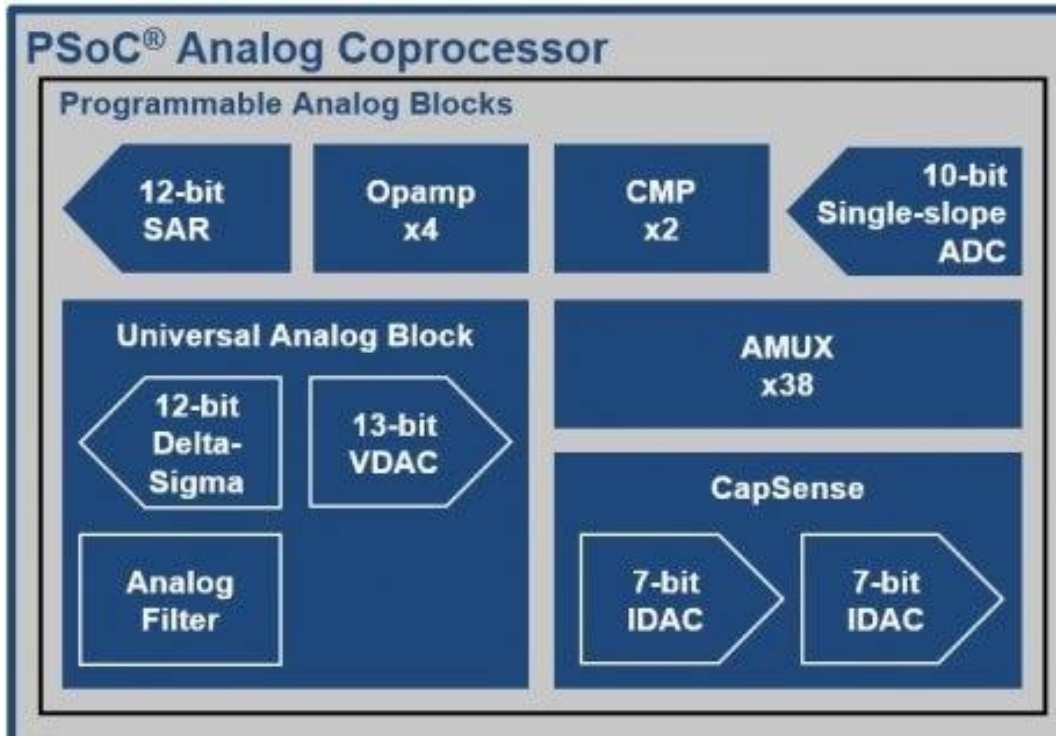
- 12-bit SAR ADC
  - Sample rate up to 1 Msps
  - Selectable resolution 8-, 10-, or 12-bit
  - Automated hardware sequencer with 16 input channels
  - Each channel can be differential or single-ended
  - Integrated hardware averaging per channel
  - Programmable input channels, for example external pins, Opamps, and UAB

Cypress PSoC Analog Coprocessor



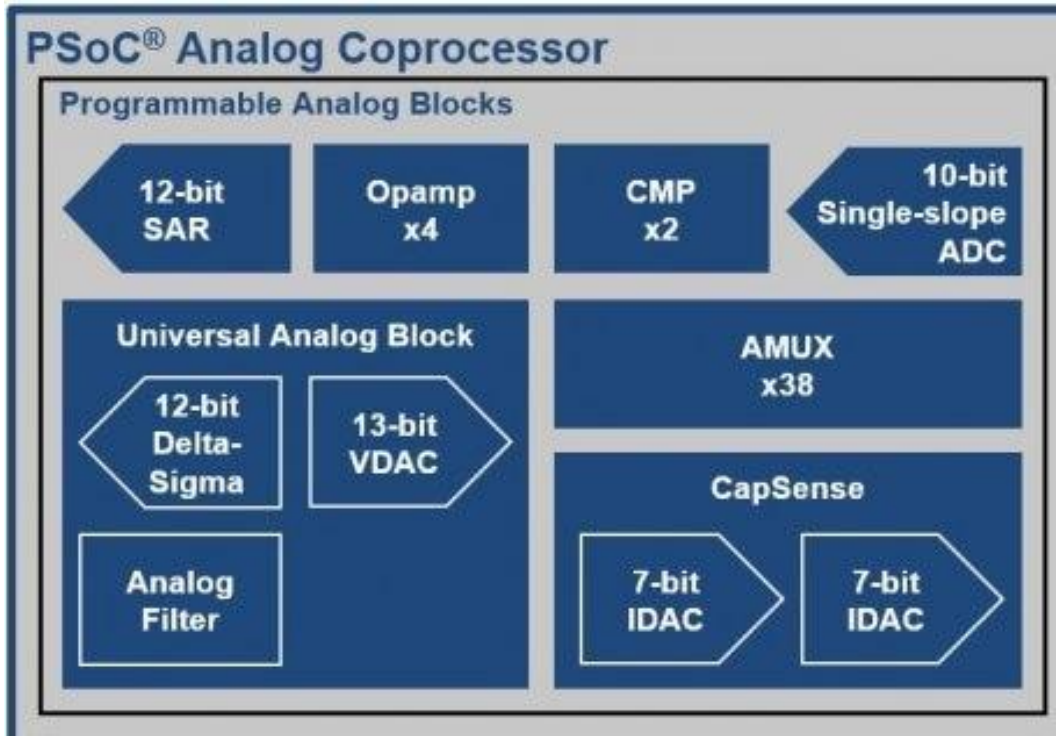
- Four programmable Opamps
  - 90 dB open-loop gain, rail-to-rail operation
  - Can be used with external components to form standard Opamp circuits
  - Can use an internal resistor array to form a programmable gain amplifier (PGA) with gain up to 32
  - 6 MHz gain-bandwidth when driving external I/Os, with up to 10 mA drive
  - 8 MHz gain-bandwidth when driving internal nodes such as the SAR ADC
  - ±1 mV input offset voltage
  - 15 µA operating current in Deep-Sleep mode

Cypress PSoC Analog Coprocessor



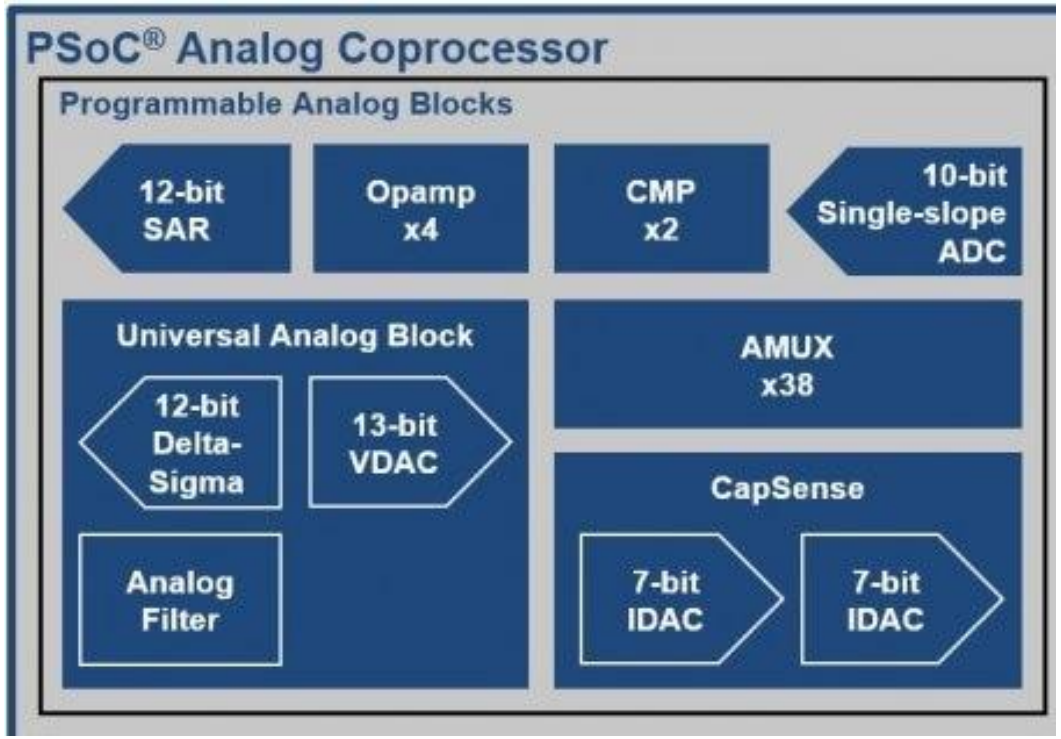
- Universal Analog Block (UAB) configurable as one of:
  - 12-bit buffered voltage DAC (VDAC), with a sample rate of 500 kHz
  - 2nd-order bi-quad filter, as a low-pass, high-pass, band-pass, or notch filter
  - 2-bit delta-sigma ADC, with a sample rate of 7.8 Ksps and a DNL of ±1 LSB
  - 14-bit incremental delta-sigma ADC, with a sample rate of 100 sps and a DNL of ±2 LSB

Cypress PSoC Analog Coprocessor



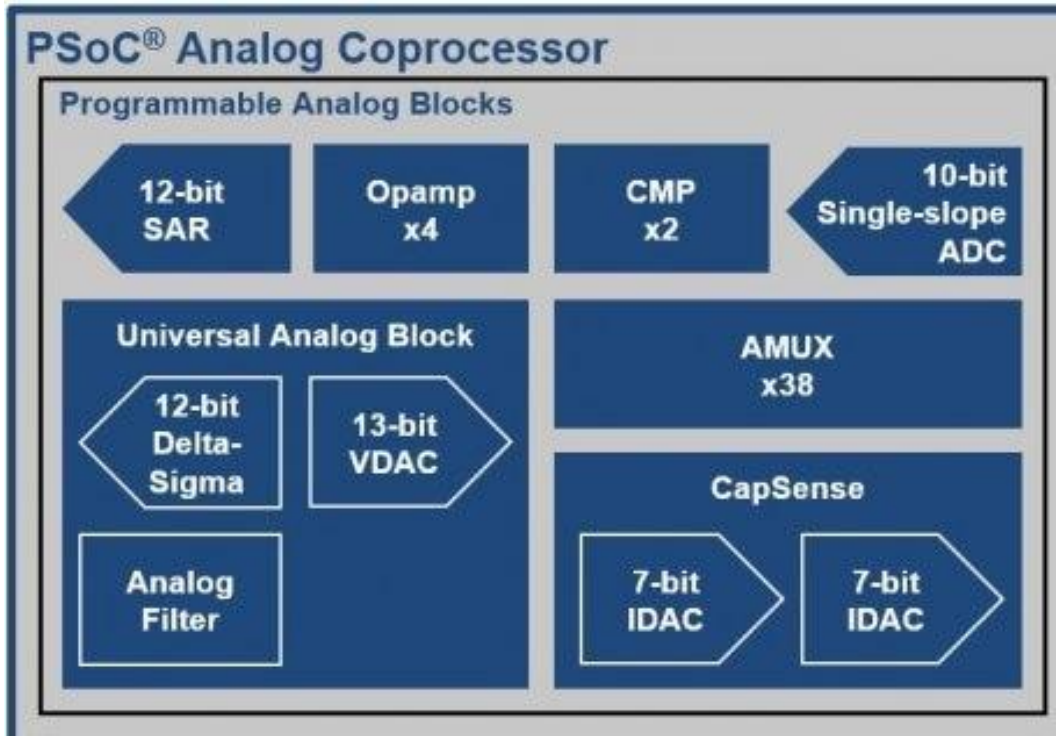
- Two low power comparators (CMP)
  - Wake up the device from low-power modes
- Single-Slope ADC
  - Selectable 8- or 10-bit resolution
  - Sample rate up to 11.6 ksps with 10-bit resolution
  - Input measurement range from V_{SS} to V_{DDA} on any GPIO pin
  - Implemented in the CapSense block

Cypress PSoC Analog Coprocessor



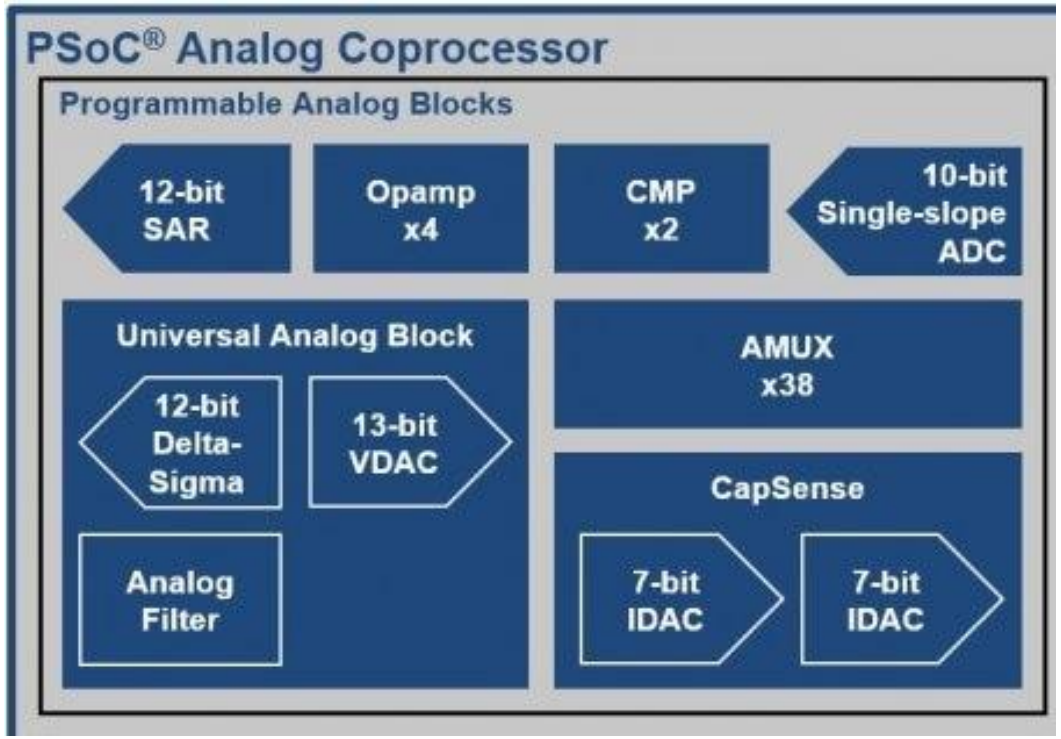
- Programmable Reference Block (PRB)
  - Four voltage references, independently adjustable in 16 steps, from V_{DDA} to V_{SS}, or 1.2 V to V_{SS}
  - References can be routed to internal high-impedance analog resources: ADC, VDAC, comparator, Opamps.
  - References can also be routed to a GPIO if buffered through an Opamp

Cypress PSoC Analog Coprocessor



- CapSense®
  - Measures capacitance; can be used with capacitive sensors, for example liquid level or touch sensing applications
  - Self and mutual capacitive sensing methods
  - Improved electromagnetic interference (EMI) using spread spectrum clock and programmable slew rate control

Cypress PSoC Analog Coprocessor



- IDACs
  - Two 7-bit current DACs (IDACs) for use with CapSense or for general purpose applications
  - A single 8-bit IDAC can be created by combining the two IDACs in parallel
  - 37.5 nA LSB current, for precise capacitance measurements
  - Six output current ranges (4.76 µA to 609 µA), in source or sink configuration

PSoC Creator Toolchain

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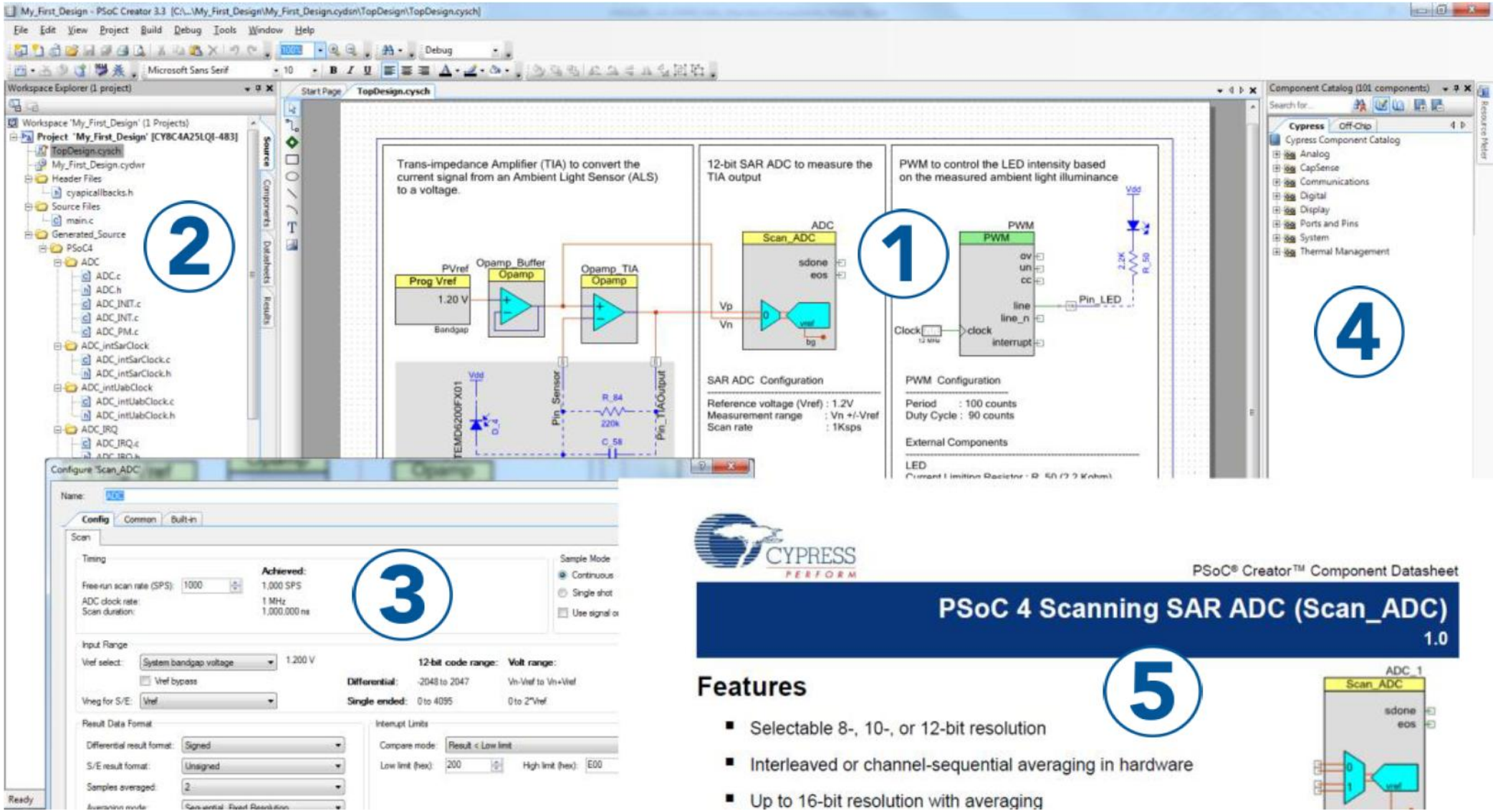
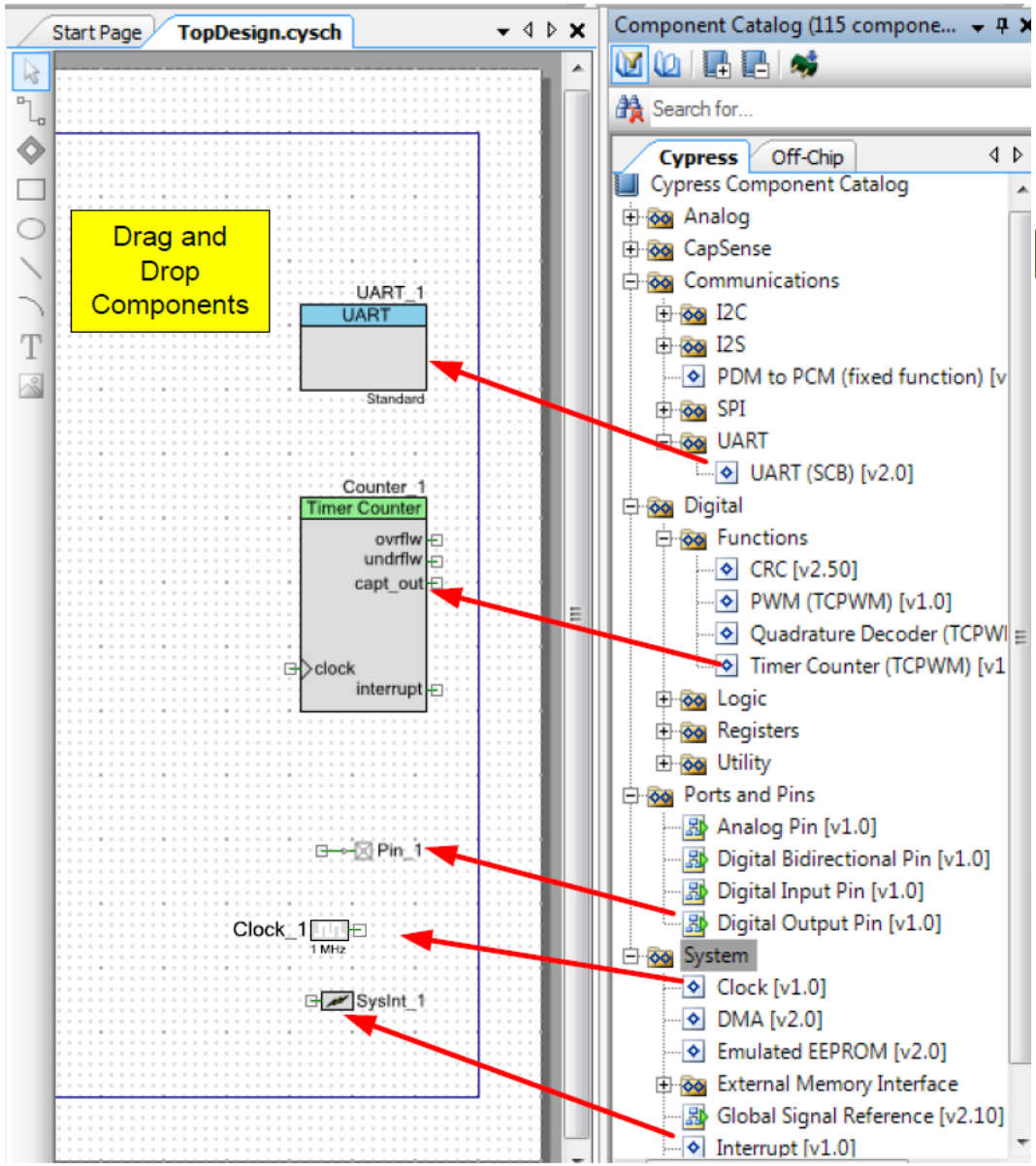
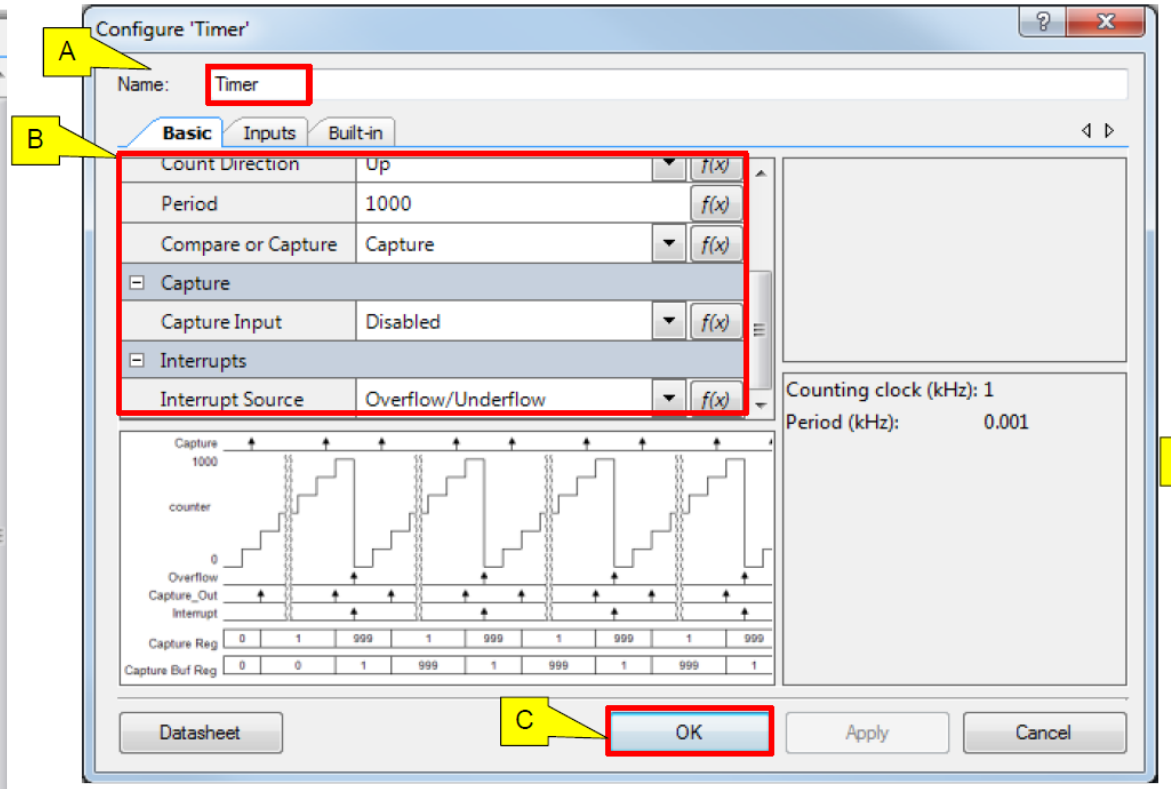
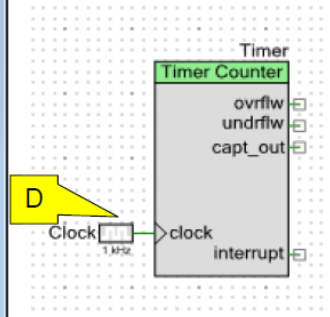
1. Drag and drop components
2. Codesign application firmware
3. Component configuration tool
4. Library of pre-designed components
5. Component datasheets




Start Page
TopDesign.cysch
Drag and Drop Components
UART_1
UART
Standard
Counter_1
Timer Counter
ovrflw
undrflw
capt_out
clock
interrupt
Pin_1
Clock_1
1 MHz
SysInt_1

Component Catalog (115 compone...
Search for...
Cypress
Off-Chip
Cypress Component Catalog
Analog
CapSense
Communications
I2C
I2S
PDM to PCM (fixed function) [v
SPI
UART
UART (SCB) [v2.0]
Digital
Functions
CRC [v2.50]
PWM (TCPWM) [v1.0]
Quadrature Decoder (TCPWI
Timer Counter (TCPWM) [v1
Logic
Registers
Utility
Ports and Pins
Analog Pin [v1.0]
Digital Bidirectional Pin [v1.0]
Digital Input Pin [v1.0]
Digital Output Pin [v1.0]
System
Clock [v1.0]
DMA [v2.0]
Emulated EEPROM [v2.0]
External Memory Interface
Global Signal Reference [v2.10]
Interrupt [v1.0]


A
Configure 'Timer'
Name:
Timer
B
Basic
Inputs
Built-in
Count Direction
Up
Period
1000
Compare or Capture
Capture
Capture
Capture Input
Disabled
Interrupts
Interrupt Source
Overflow/Underflow
Counting clock (kHz): 1
Period (kHz): 0.001
Datasheet
C
OK
Apply
Cancel


D
Timer
Timer Counter
ovrflw
undrflw
capt_out
Clock
1 kHz
clock
interrupt

Example PSoC Application

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AN73468

PSoC® 3 and PSoC 5LP - Single-Cell Lithium-Ion (Li-ion) Battery Charger

Author: Archana Yarlagadda, Rajiv Badiger
Associated Project: Yes
Associated Part Family: All PSoC 3 and PSoC 5LP Parts
Software Version: PSoC® Creator™ 3.0 or Higher
Related Application Notes: AN55102

AN73468 explains a single-cell Lithium-Ion (Li-ion) battery charger implementation using PSoC 3 or PSoC 5LP. Two types of implementations — linear and switching type are supported. An attached PSoC Creator project, which includes a charge display tool, demonstrates Li-ion battery charging.

Figure 1. Charge Profile for Li-ion Battery

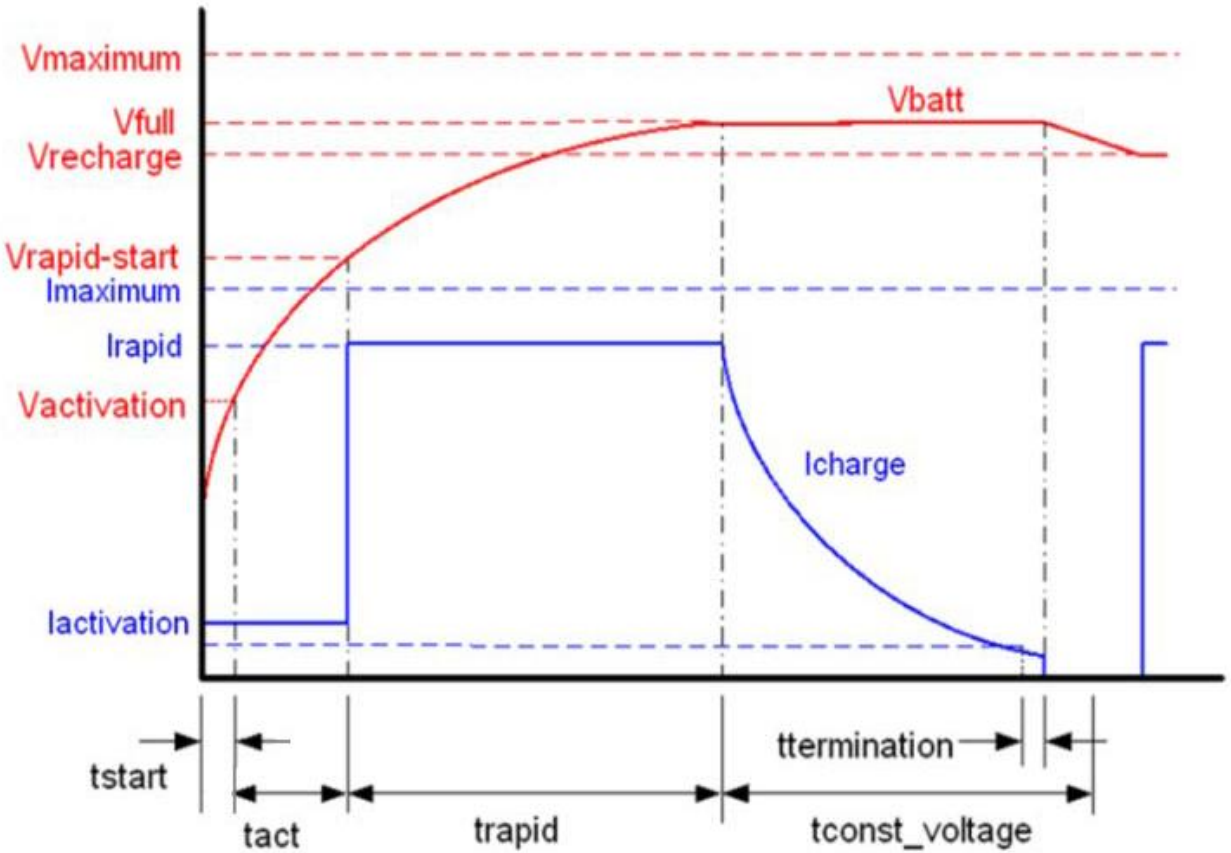

Figure 2. Block Diagram of Battery Charger

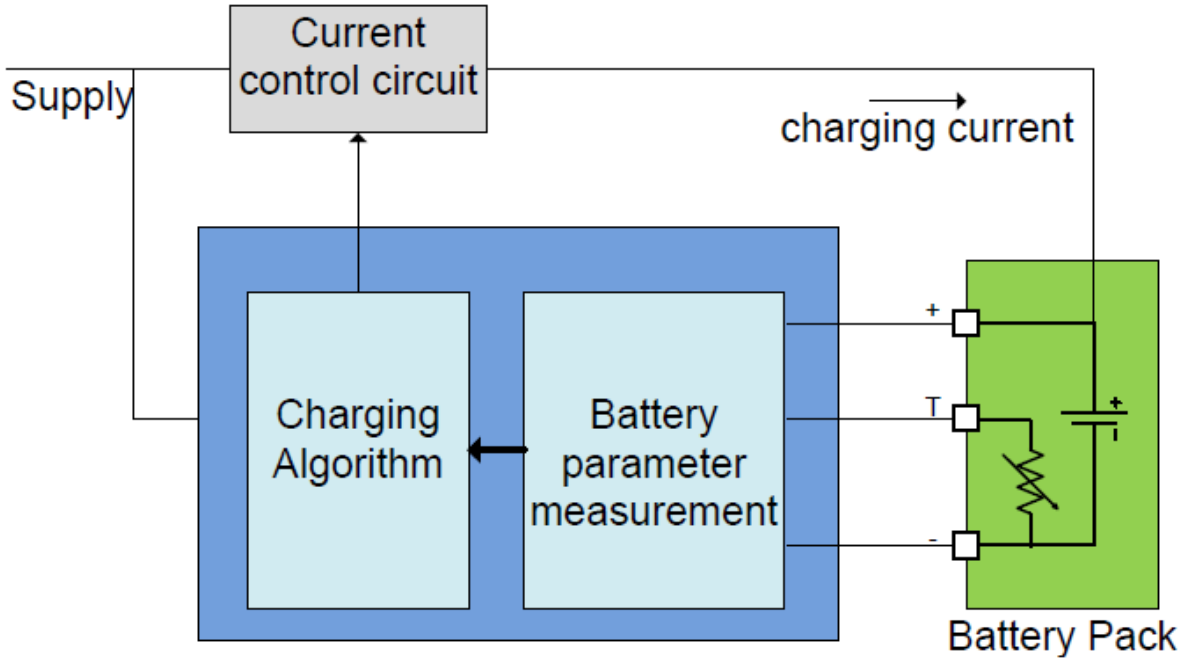

Figure 3. Block Diagram for Li-ion Battery Charger with PSoC