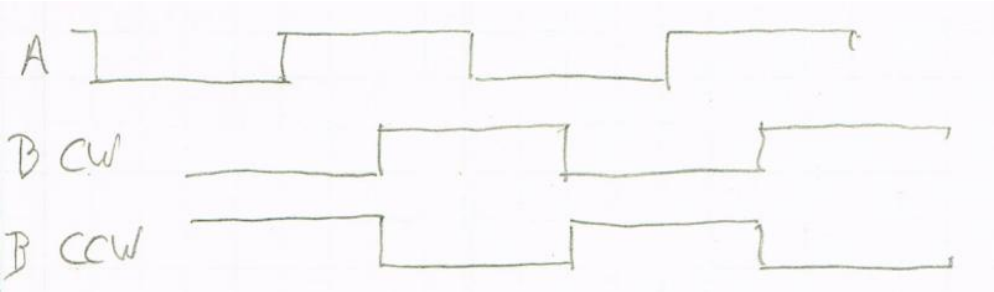
F2025 ECE 460/560: ESA THW1 Solutions

Shaft Rotation Position Decoder

A quadrature encoder generates two digital output signals (A, B) as a shaft rotates, as described in class. Each signal generates 90 pulses per full revolution of the shaft. A and B are phase-shifted by 90 degrees. Determining rotation direction requires decoding signals A and B as follows.

- For clockwise shaft rotation, signal B will be 0 every time signal A rises from 0 to 1. B will be 1 every time A falls from 1 to 0.
- For counter-clockwise shaft rotation, B will be 1 every time A rises from 0 to 1. B will be 0 every time A falls from 1 to 0.



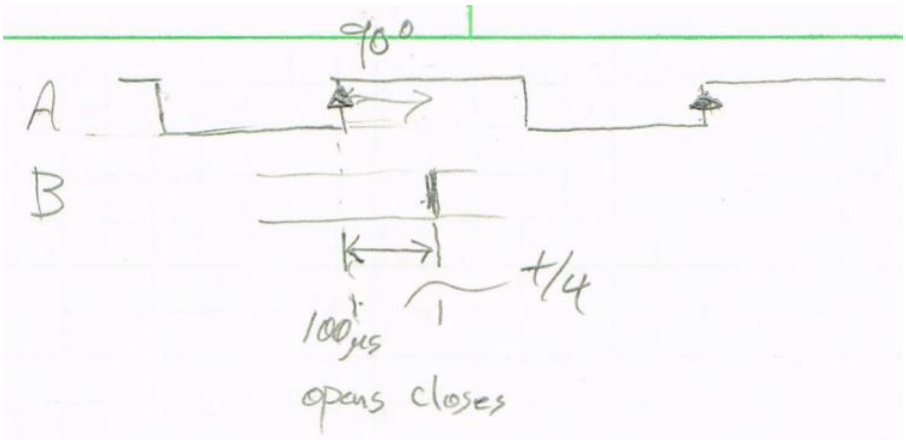
Q1. 5 pts

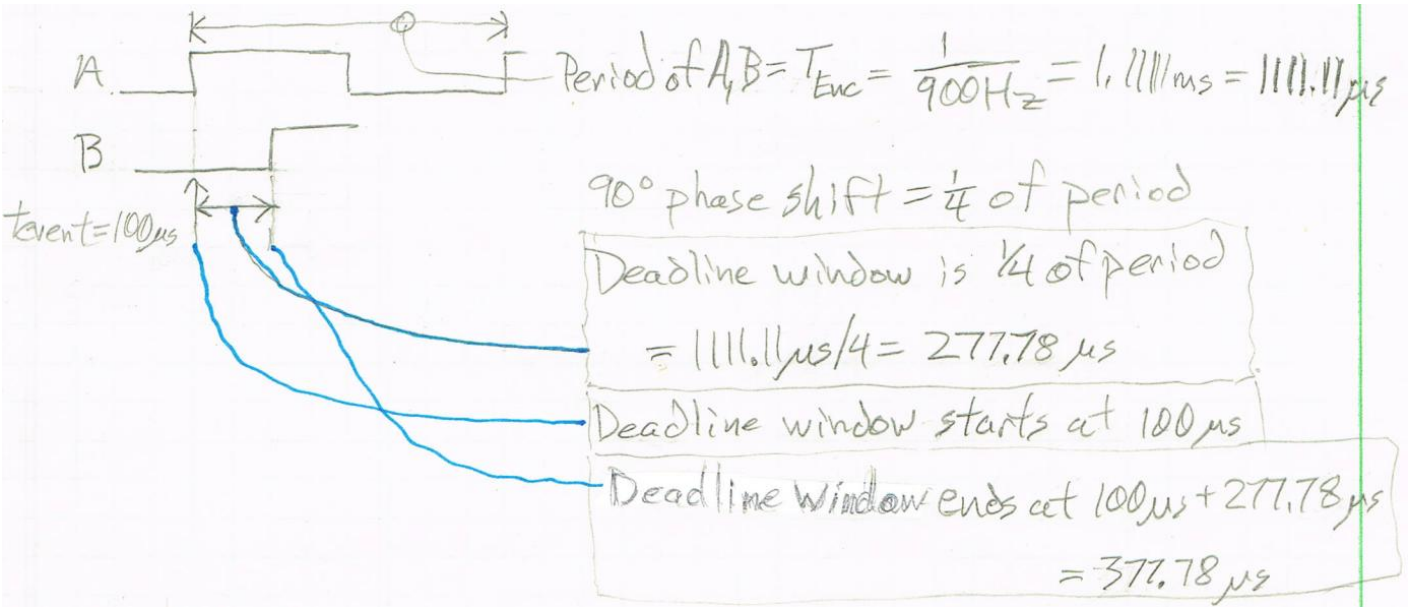
What is the frequency of the signal A when the shaft is rotating at 10 Hz?

900 Hz

Q2. 5 pts

Assume the shaft is rotating at 10 Hz and A rises from 0 to 1 at t_event = 100 microseconds. For a correct position update (+ vs. -), when is the deadline window for the decoder to read the B signal? (e.g. Window opens at 144 microseconds, closes at 8513 microseconds) *





Opening time: 100 us
Closing time: 378 us (377.777... us)

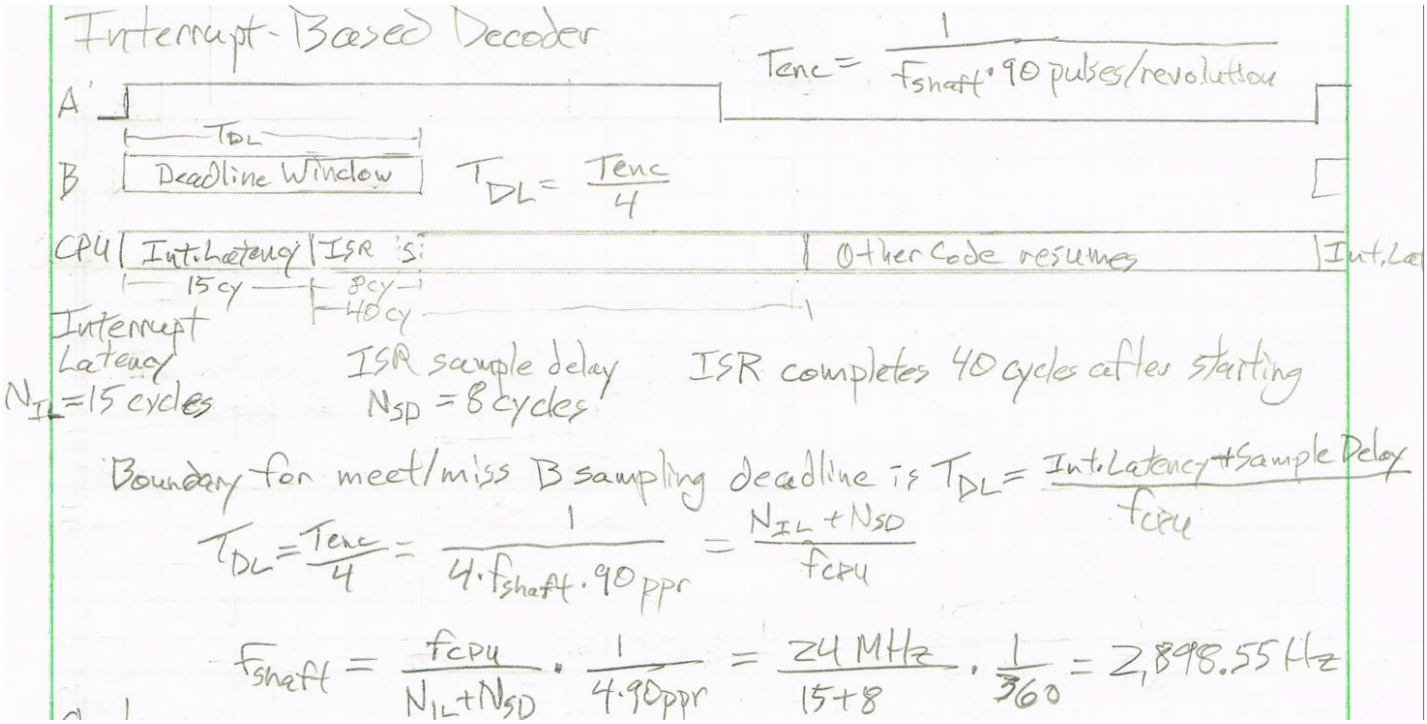
Interrupt-Based Decoder

For the following questions, consider a decoder with the following characteristics:

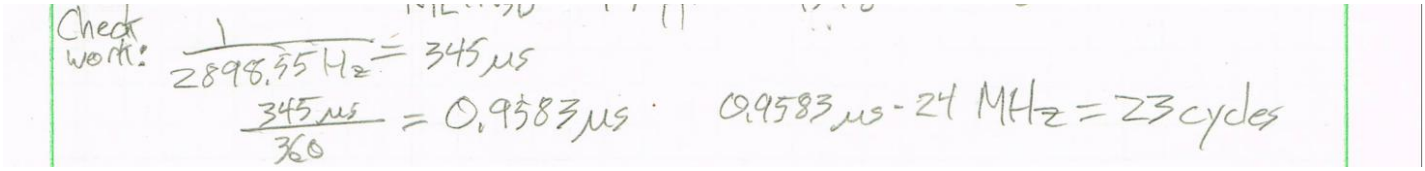
- A port/GPIO peripheral monitors signal A and generate an interrupt request for each rising edge of A. The corresponding interrupt service routine (ISR) reads B, determines rotation direction, and either increments or decrements the variable (an integer) storing the measured shaft position.
- The CPU is running at 24 MHz.
- The CPU's interrupt latency (from interrupt request to first instruction of ISR starting to execute) is 15 CPU clock cycles. During this time, the CPU is not executing any instructions.
- The ISR reads signal B eight cycles after the ISR starts executing.

Q3. 5 pts

For this interrupt-based decoder, what is the maximum possible shaft rotation speed? Assume that the total ISR duration is 40 CPU clock cycles, and no other CPU processing needs to be done. Explain your approach and show your work. *



Optional: Checking the result



- Frequency: 2.5 pts
  - Full Credit: 2898.55… Hz, 2899 Hz, 2900 Hz
  - Partial Credit:
    - Off by a factor of 2
    - Off by a factor of 4
- Explanation: 2.5 pts. Key Concepts/Steps
  - At what shaft frequency is the sample taken at the end of the deadline window? (Boundary case)
    - Set the two deadline window equations equal to each other
      - From shaft rotation and encoder: $T_{DL} = (¼) * (1/(f_{shaft} * N_{PPR}))$
      - From CPU: T_{DL} = (Interrupt latency + delay to read signal B)/CPU clock frequency = (15 cy + 8 cy)/f_{cpu}
    - Solve for f_{shaft}
- Extra credit for confirming timing feasibility: 1 pt. At that shaft frequency, is there enough time for the CPU to respond to the interrupt and run the decoder?
  - ISR finishes (40 + 15 cycles)/24 MHz after triggering = 55/24 MHz = 2.29 us
  - Period of encoder signal Tenc = 3.83 us
  - Yes, there is enough time since 2.29 us < 3.83 us

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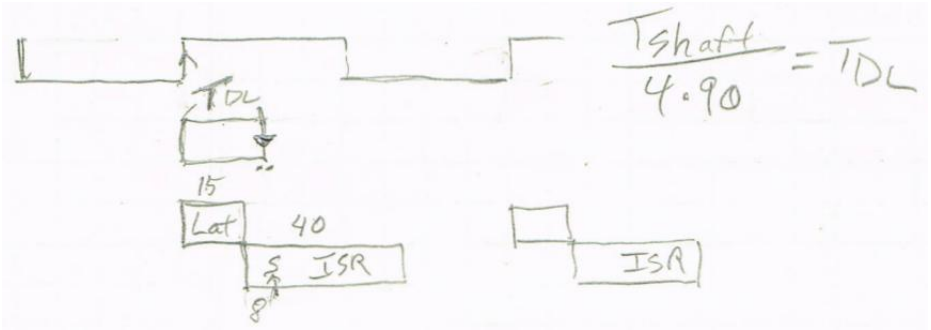
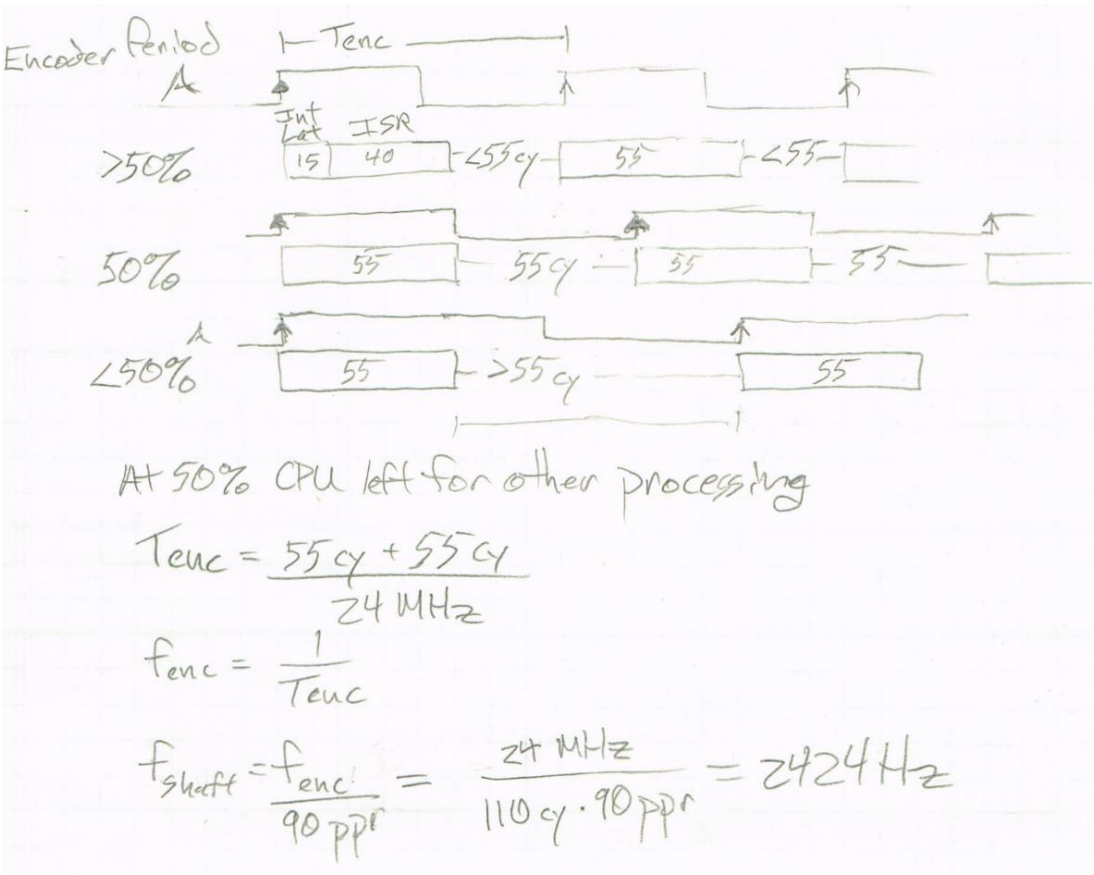
Q4. 5 pts

Consider the interrupt-based decoder above. Assume that we want to leave 50% of the CPU time for other processing. What is the maximum possible shaft rotation speed? Explain your approach and show your work.





- Frequency: 2.5 pts
  - Full Credit: 2424.2424…. Hz, 2424 Hz
- Explanation: 2.5 pts. At what shaft frequency is 50% of the CPU time available? Key Concepts/Steps
  - The decoder uses CPU time for two activities:
    - Executing the ISR (40 CPU clock cycles)
    - Perform the hardware interrupt response operations (15 CPU clock cycles). No instructions are executed at this time.
  - Splitting the CPU time 50% between the decoder and other processing gives 55 cycles for the decoder and 55 cycles for the other work.
  - To get this 50% time split, the decoder must be triggered every 110 cycles (T_{Enc}).
  - Convert this 110 cycle period to a decoder triggering frequency: 24 MHz/110 cycles

- Divide this frequency by 90 pulses per revolution to get the shaft frequency